AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A semiconductor memory device comprising:

an SDRAM array made up of a plurality of memory cells and having an information bit area whereininformation bits are written in and / or read from and a parity bit area whereinparity bits are written in and / or read from, and a redundant circuit to replace error bits contained in at least one of said information bits and said parity bits; and

an error correcting code (ECC) circuit to perform error correcting processing, using a Hamming Code on data including said information bits and said parity bits being written in and /or read from said information bit area and said parity bit area, respectively, in said SDRAM array,

wherein use of redundant correcting processing to correct said error bits using a redundant circuit in said SDRAM array is combined with said error correcting processing using said Hamming Code in said error correcting code (ECC) circuit, and

wherein said error correcting code circuit comprises a plurality of divided error correcting code circuits provided independently of each other for each independent data mask block and controlled by a-independent data mask signal-signals as an-external signalsignals.

2. (previously presented): The semiconductor memory device according to Claim 1, wherein, when reading processing is performed on said information bit area or said parity bit

area, said data on which said error correcting processing has been performed is output to only an outside of said SDRAM array without being rewritten into said information bit area or said parity area.

3. (previously presented): The semiconductor memory device according to Claim 1, wherein, when a codeword made up of bits occurs which is beyond a correcting capability of said error correcting processing using said Hamming Code, said redundant correction processing is performed on said error bits using said redundant circuit.

4. (original): The semiconductor memory device according to Claim 1, wherein said error correcting code (ECC) circuit comprises an encoding circuit to output, by arithmetic operations, said parity bit corresponding to said information bit, a decoding circuit to output an error location detecting signal indicating an error bit out of all bits contained in said codeword, and an error correcting circuit to input said error location detecting signal and to output an error bit in a reverse manner.

5. (original): The semiconductor memory device according to Claim 4, wherein said encoding circuit comprises a syndrome tree in which a plurality of AND circuits to which a first test signal is fed is connected to a plurality of exclusive OR circuits in a manner to provide a specified relationship.

6. (original): The semiconductor memory device according to Claim 4, wherein said decoding circuit comprises a syndrome tree in which a plurality of exclusive OR circuits is connected to one another so that a plurality of bits of said information bits and a plurality of bits of said parity bits are input and a plurality of bits of syndromes is output and decoders to which a plurality of NAND circuits to which a plurality of bits of said syndromes is input and in which a plurality of bits of said error location detecting signals are output and a plurality of AND circuits to which a second test signal is fed are connected to one another in a manner to provide a specified relationship.

7. (original): The semiconductor memory device according to Claim 4, wherein, in said error correcting circuit, a plurality of exclusive OR circuits to which a plurality of bits of said error location detecting signals is input together with a plurality of bits of said information bits and a plurality of bits of said parity bits and a plurality of switches to which a third test signal is fed are connected to one another in a manner to provide a specified relationship so that said error bits are output in a reverse manner.

8. (canceled).

9. (currently amended): A semiconductor memory device comprising:

an SDRAM array made up of a plurality of memory cells and having an information bit area whereininformation bits are written in and / or read from and a parity bit area wherein parity bits are written in and / or read from, and a redundant circuit to replace error bits contained in at least one of said information bits and said parity bits; and

an error correcting code (ECC) circuit to perform error correcting processing, using a Hamming Code whose code length is 72 or less on data including said information bits and said parity bits being written in and /or read from said information bit area and said parity bit area, respectively, in said SDRAM array,

wherein use of redundant correcting processing to correct said error bits using a redundant circuit in said SDRAM array is combined with said error correcting processing using said Hamming Code in said error correcting code (ECC) circuit, and

wherein said error correcting code circuit comprises a plurality of divided error correcting code circuits provided independently of each other for each independent data mask block and controlled by a-independent data mask signal-signals as an-external signalsignals.

10. (previously presented): The semiconductor memory device according to Claim 9, wherein, when reading processing is performed on said information bit area or said parity bit area, said data on which said error correcting processing has been performed is output to only an outside of said SDRAM array without being rewritten into said information bit area or said parity area.

11. (previously presented): The semiconductor memory device according to Claim 9, wherein, when a codeword made up of bits occurs which is beyond a correcting capability of said error correcting processing using said Hamming Code, said redundant correction processing is performed on said error bits using said redundant circuit.

12. (original): The semiconductor memory device according to Claim 9, wherein said error correcting code (ECC) circuit comprises an encoding circuit to output, by arithmetic operations, said parity bit corresponding to said information bit, a decoding circuit to output an error location detecting signal indicating an error bit out of all bits contained in said codeword, and an error correcting circuit to input said error location detecting signal and to output an error bit in a reverse manner.

13. (original): The semiconductor memory device according to Claim 12, wherein said encoding circuit comprises a syndrome tree in which a plurality of AND circuits to which a first test signal is fed is connected to a plurality of exclusive OR circuits in a manner to provide a specified relationship.

14. (original): The semiconductor memory device according to Claim 12, wherein said decoding circuit comprises a syndrome tree in which a plurality of exclusive OR circuits is connected to one another so that a plurality of bits of said information bits and a plurality of bits of said parity bits are input and a plurality of bits of syndromes is output and decoders to which a plurality of NAND circuits to which a plurality of bits of said syndromes is input and in which a

plurality of bits of said error location detecting signals are output and a plurality of AND circuits to which a second test signal is fed are connected to one another in a manner to provide a specified relationship.

15. (original): The semiconductor memory device according to Claim 12, wherein, in said error correcting circuit, a plurality of exclusive OR circuits to which a plurality of bits of said error location detecting signals is input together with a plurality of bits of said information bits and a plurality of bits of said parity bits and a plurality of switches to which a third test signal is fed are connected to one another in a manner to provide a specified relationship so that said error bits are output in a reverse manner.

16. (canceled).